Amendments to the Claims

Please amend claims 3-8 and 10-16 as shown below.

Listing of Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently amended) Nonvolatile two-transistor semiconductor memory cell comprising ~~having~~

a memory transistor (ST) having a predetermined threshold voltage, which has a source and drain region (2) with a channel region lying in between in a substrate (1), a first memory transistor insulation layer (3), a charge storage layer (4), a second memory transistor insulation layer (5) and a memory transistor control layer (6) being formed at the surface of the channel region; and

a selection transistor (AT) having a predetermined threshold voltage, which has a source and drain region (2) with a channel region lying in between in the substrate (1), a first selection transistor insulation layer (3') and a selection transistor control layer (4*) being formed at the surface of the channel region, characterized in that

the two threshold voltages in the selection and memory transistors (AT, ST) are raised by an increased substrate/well doping and, for correction of the threshold raising in the selection transistor (AT), the selection transistor control layer (4*) is formed differently from the charge storage layer (4).

2. (Original) Nonvolatile two-transistor semiconductor memory cell according to Patent Claim 1,

characterized in that

the selection transistor control layer (4*) and the charge storage layer (4) have a different material and/or a different doping.

3. (Currently amended) Nonvolatile two-transistor semiconductor memory cell according to Patent Claim 1 [[or 2]],

characterized in that

the substrate (1) has a semiconductor material with a doping of the first conduction type (p),

the selection transistor control layer (4*) has a semiconductor material with a doping of the first conduction type (p), and the charge storage layer (9) has a semiconductor material with a doping of the second conduction type (n), which doping is opposite to the first conduction type.

4. (Currently amended) Nonvolatile two-transistor semiconductor memory cell according to ~~one of~~ Patent Claim 1 ~~Claims 1 to 3~~,

characterized in that the dopant concentration of the first conduction type (p) is increased in the substrate (1), the channel regions or a well region.

5. (Currently amended) Nonvolatile two-transistor semiconductor memory cell according to one of Patent Claim 1 ~~Claims 1 to 4~~,

characterized in that the first memory transistor insulation layer (3) and the first selection transistor insulation (3') have an SiO_2 layer.

6. (Currently amended) Nonvolatile two-transistor semiconductor memory cell according to one of Patent Claim 1 ~~Claims 1 to 5~~,

characterized in that the charge storage layer (9) and the selection transistor control layer (9*) have a polysilicon layer and/or a metallic layer.

7. (Currently amended) Nonvolatile two-transistor semiconductor memory cell according to one of Patent Claim 1 ~~Claims 1 to 6~~,

characterized in that the memory transistor (ST) and the selection transistor (AT) represent an NMOS and/or a PMOS transistor.

8. (Currently amended) Method for fabricating a nonvolatile two-transistor semiconductor memory cell, the method comprising ~~having the following steps~~:

a) formation of a first insulation layer (3, 3') for a selection transistor (AT) having a predetermined threshold voltage and a memory transistor (ST) having a predetermined threshold voltage on a semiconductor substrate (1), which has a doping of the first conduction type (p);

b) formation of a semiconductor layer (4) at the surface of the first insulation layer (3, 3');

c) formation of a second insulation layer (5) at the surface of the electrically conductive semiconductor layer (4) at least in the region of the memory transistor (ST);

d) formation of a further electrically conductive layer (6) at the surface of the second insulation layer (5) at least in the region of the memory transistor (ST);

e) formation and patterning of a mask layer (7);

f) formation of layer stacks in the region of the selection transistor (AT) and of the memory transistor (ST) using the patterned mask layer (7); and

g) formation of source and drain regions (2) with a doping of the second conduction type (n) using the layer stack as mask, in which case in step a), the two threshold voltages in the selection and memory transistors (AT, ST) are raised by an increased doping of the semiconductor substrate (1), and

in step b), for correction of the threshold raising in the selection transistor (AT), the semiconductor layer has a doping of the first conduction type (p) in a region of the selection transistor (AT) and a doping of the second conduction type (n), which doping is opposite to the first conduction type, in a region of the memory transistor (ST).

9. (Original) Method according to Patent Claim 8,

characterized in that, in step a), a semiconductor substrate (1) with increased basic doping, well doping and/or surface doping of the first conduction type (p) is used.

10. (Currently amended) Method according to ~~either of~~ Patent Claim 8 ~~Claims 8 or 9~~,

characterized in that, in step a), a tunnel oxide layer (TOX) is formed in the region of the memory transistor (ST) and a gate oxide layer (GOX) is formed in the region of the selection transistor (AT).

11. (Currently amended) Method according to ~~one of~~ patent Claim 9 ~~Claims 9 to 10~~,

characterized in that, in step b), a polysilicon layer is deposited and the different doping in the region of the selection transistor (AT) and of the memory transistor (ST) is effected by a masked implantation.

12. (Currently amended) Method according to ~~one of~~ Patent Claim 9 ~~Claims 9 to 11~~,

characterized in that, in step c), an ONO layer sequence is formed.

13. (Currently amended) Method according to ~~one of~~ Patent Claim 9 ~~Claims 9 to 12~~,

characterized in that, in step d), a further polysilicon layer is deposited, which has a doping of the second conduction type (n).

14. (Currently amended) Method according to ~~one of~~ Patent Claim 9 ~~Claims 9 to 13~~,

characterized in that, in step e), a hard mask layer is formed.

15. (Currently amended) Method according to ~~one of~~ Patent Claim 9 ~~Claims 9 to 14~~,

characterized in that, in step f), an anisotropic etching method is carried out.

16. (Currently amended) Method according to ~~one of~~ Patent Claim 9 ~~Claims 9 to 15~~,

characterized in that, in step g), an ion implantation (I) is carried out.